

CLAIMS

- 1 1. A CMOS bus hold circuit defining an input and an output, the bus hold circuit
2 powered from a positive power rail, V_{cc} , the bus hold circuit comprising:
3 a first inverter receiving an input signal, V_{in} , at the input and providing its com-
4 plement at the output,
5 an arbiter circuit arranged to selectively connect the more positive of V_{in} or V_{cc}
6 to a pseudo power rail or prail,
7 a second inverter receiving the output and providing its complement back to the
8 input thereby latching or holding the logic state of V_{in} , the second inverter defining a
9 power connection,
10 a PMOS transistor arranged, when on, to connect the power connection to V_{cc} ,
11 and when off to disconnect the second inverter from V_{cc} , thereby allowing the power
12 connection to float, and where the PMOS N-well is connected to the prail, thereby pre-
13 venting the PMOS drain to N-well from being forward biased,
14 a comparator circuit arranged to receive and compare V_{in} to V_{cc} , and provide a
15 control signal equal to V_{in} when the V_{in} is higher than V_{cc} , and to disconnect the control
16 signal, allowing it to float, when V_{cc} is higher than V_{in} , and
17 a switch that is on and pulls the control signal low when V_{in} is a logic low, and
18 where the switch is off when V_{in} is not a logic low,
19 wherein the bus hold circuit draws no DC current, and where when V_{in} is higher
20 than V_{cc} no leakage current is drawn from V_{in} .
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- 1 2. The bus hold circuit of claim 1 wherein the arbiter circuit comprises two PMOS
2 transistors with their drains and N-wells connected together.
- 1 3. The bus hold circuit of claim 1 wherein the switch is a PMOS transistor with its
2 gate connected to V_{in} and its source connected to the control signal.

1 4. The bus hold circuit of Claim 1 wherein the comparator comprises:
2 a first PMOS with its source connected to V_{in} and its gate connected to V_{cc} ,
3 a second PMOS with its source connected to the drain of the first PMOS and its
4 gate connected to V_{cc} , and its drain connected to the control signal,
5 a third PMOS with its source connected to the source of the second PMOS and its
6 gate connected to V_{in} ,
7 wherein the N-wells of the first, second, and third PMOS transistors are all con-
8 nected to the prail,
9 a first NMOS with its drain connected to the drain of the second PMOS and its
10 source connected to a power return,
11 a second NMOS with its drain connected to the drain of the third PMOS, its gate
12 connected to its drain and to the gate of the first NMOS, and its source connected to the
13 power return, wherein the first, second, and third PMOS transistors and the first and sec-
14 ond NMOS transistors form a comparator circuit wherein the control signal is connected
15 to V_{in} when V_{in} is higher the V_{cc} , and where the control signal is unconnected and floats
16 when V_{cc} is higher than V_{in} , and further wherein the comparator uncertainty when V_{in}
17 and V_{cc} are near each other is limited to differential of about 100 millivolts.

1 5. A bus hold circuit defining an input and an output, the bus hold circuit powered
2 from a positive power rail, V_{cc} , the bus hold circuit comprising:
3 means for receiving an input signal, V_{in} , at the input and providing its comple-
4 ment at the output,
5 means to selectively connect the more positive of V_{in} or V_{cc} to a pseudo power
6 rail or prail,
7 inverter means for receiving the output and providing its complement back to the
8 input thereby latching or holding the logic state of V_{in} ,
9 means for connecting and disconnecting the inverter means to V_{cc} , wherein when
10 disconnected the inverter means floats,

11 means for comparing V_{in} to V_{cc} , and for providing a control signal equal to V_{in}
12 when the V_{in} is higher than V_{cc} , and for disconnecting the control signal, allowing it to
13 float, when V_{cc} is higher than V_{in} , and
14 means for pulling the control signal low when V_{in} is a logic low,
15 wherein the bus hold circuit. draws no DC current, and when V_{in} is higher than
16 V_{cc} no leakage current is drawn from V_{in} .

1 6. A process for holding an input bus signal and outputting the signal or its comple-
2 ment, the process comprising the steps of:
3 receiving an input signal, V_{in} , at an input and providing its complement,
4 selectively connect the more positive of V_{in} or V_{cc} to a pseudo power rail or
5 prail,
6 receiving the output and providing its complement back to the input thereby de-
7 fining an inverter for latching or holding the logic state of V_{in} ,
8 connecting and disconnecting the inverter to V_{cc} , wherein when disconnected the
9 inverter means floats,
10 comparing V_{in} to V_{cc} , and providing a control signal equal to V_{in} when the V_{in}
11 is higher than V_{cc} , and for disconnecting the control signal, allowing it to float, when
12 V_{cc} is higher than V_{in} , and
13 pulling the control signal low when V_{in} is a logic low,
14 configuring the process to draw no DC current and no leakage current when V_{in}
15 is higher than V_{cc} .

1 7. A computer system including one or more of the bus hold circuits defined in
2 Claim 1.